REMARKS

Claims 1-19 are pending in the present application, were examined, and stand rejected. In response to the Examiner's Answer, Claims 1, 10 and 18-19 are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-19 and withdrawal of the rejections of record in view of such amendments and the following remarks.

I. Claims Rejected Under 35 U.S.C. §102

The Patent Office rejected Claims 1-5, 7-13 and 15-19 under 35 U.S.C. §102(b) as being taught by U.S. Patent No. 5,685,009 issued to Blomgren, et al. ("Blomgren1") and U.S. Patent No. 5,781,750 issued to Blomgren, et al. ("Blomgren2"). Applicants respectfully traverse this rejection.

Regarding Claim 1, Claim 1 is amended to recite the following claim feature which is not disclosed by Blomgren1 and Blomgren2:

> a first instruction set engine to process instructions from a first instruction set architecture (ISA), the first ISA having a first word size;
> a second instruction set engine to process instructions from a second ISA, the second ISA having a second word size, the second word size being different than the first word size. (Emphasis added.)

As indicated by the Examiner's Answer, the claim language of Claim 1 can be interpreted as follows:

> The first interpretation, as shown in Diagram 1 below, has the language of "a first instruction set architecture (ISA)" modifying the instructions being processes by a first instruction set engine and the "having a first word size" modifying the first ISA. The second interpretation, as shown in Diagram 2 below, has both the language of "a first instruction set architecture (ISA)" and "having a first word size" modifying the instructions being processes by a first instruction set engine. (See pp. 26, ¶ 2 of the Examiner's Answer mailed 04/18/06.) (Emphasis added.)

As indicated by the Examiner's Answer, the Examiner interprets the Claim 1 according to the second interpretation. (See supra.) In response, Applicants amend Claim 1

such that the phrase "having a first word size" solely modifies "the first ISA" to avoid the Examiner's interpretation of Claim 1 by amending Claim 1 as follows:

> a first instruction set engine to process instructions from a first instruction set architecture (ISA), the first ISA having a first word size. (Emphasis added.)

In addition, the Applicants further amend Claim 1 such that the phrase "having a second word size" solely modifies "the second ISA" to avoid the Examiner's interpretation of Claim 1 by amending Claim 1 as follows:

> a second instruction set engine to process instructions from a second ISA, the second ISA having a second word size, the second word size being different than the first word size. (Emphasis added.)

The Examiner's Answer cites Graf's Modern Dictionary of Electronics 6th Edition © 1984 ("Graf") to provide definitions for the terms "word" and "word size." Graf defines the term "word size" as "the number of decimals or binary bits comprising a word." As indicated by the Examiner, Graf defines the term "word" as "the number of bits needed to represent a computer instruction, or the number of bits needed to represent the largest data element normally processed by a computer." (See Graf, p. 1132.) However, a relevant definition of the term "word" is provided by Graf as follows:

> 9. A group of bits handled as a unit by a digital computer, generally comprising the largest such group handled throughout the central processor as a single unit. The word length (number of bits per word) varies between computer types (e.g., 12 to 16 bits for minicomputers, 32 to 36 bits for large-scale computers). Not to be confused with byte. (See p. 1132.) (Emphasis added.)

As indicated by the passages cited above, a "word" represents a group of bits handled as a single unit by a digital computer; namely the largest such group handled throughout the central processor as a single unit. Similarly, the previous definition of "word size" provided by the Computer Dictionary Online, as cited by the Applicants in response to the Office Action mailed November 4, 2003, is defined as "the number of bits that a CPU can process at one time." This definition of "word size," when interpreted as the largest number of bits

that a CPU can process at one time, coincides with the above definition of "word" provided above by Graf.

Moreover, Applicants' Specification provides the following definition for an instruction set architecture as follows:

> A processor's instruction set and how the instruction set is used to achieve a certain result are referred to as the processor's instruction set architecture ("ISA"). The processor's ISA also necessarily describes much of the processor's internal architecture. The assembly language instructions of a processor's instruction set internally access data of a defined size commonly known as a word. The word size of a processor is defined by the processor's ISA. (See p. 1, lines 16-21 of Applicants' Specification.) (Emphasis added.)

As indicated in the cited passages above, the "words size" of a processor is defined by the processor's ISA based on the assembly language instructions, which access data according to a defined size referred to as a word. Similarly, Claim 1 recites a processor. In addition, the above definition of a "word" is provided by Graf with reference to the central processor of a digital computer. Likewise, regarding the size of such word, the size of such word, as defined by Computer Dictionary Online, refers to the number of bits that a CPU can process at one time.

Hence, the definitions of both Graf and the Computer Online Dictionary relied on by Applicants are directed to a processor as recited by amended Claim 1. Conversely, Graf's definition of the term "word," relied by the Examiner (defined as the number of bits needed to represent a computer instruction,) does not coincide with the definitions of both Graf and the Computer Online Dictionary relied on by Applicants' definition. Specifically, the definitions of Graf and the Computer Dictionary Online relied on by Applicants are provided with reference to a processor, as recited by amended Claim 1.

Accordingly, since the above definition of "word" is provided by Graf with reference to a central processor of a digital computer and the above definition of "word size" is provided by the Computer Dictionary Online with reference to a CPU, the meaning of the term "word size" as recited by the processor of amended Claim 1, to one of ordinary skill in the art of computer architecture design, at the time of the invention, is the largest number of

bits that can be processed by a processor as a single unit. Hence, the meaning of the term "word size" to one of ordinary skill in the art of computer architecture design, at the invention, would not include "instruction size,' as suggested by the Examiner. Accordingly, the Examiner's interpretation of the term "word size" as indicating an "instruction size" is unreasonable and unduly broad since the interpretation ignores the plain meaning of the term to one of ordinary skill in the art of computer architecture design at the time of the invention. (See MPEP §2111.01.)

Hence, Applicants submit that the Examiner is improperly equating the term "instruction size" with the term "word size," as recited by amended Claim 1. Based on the definitions provided above by the Computer Dictionary Online and Graf, the term "word size" in the context of a processor, as recited by Claim 1, refers to the largest number of bits that a processor can process as a single unit (at one time.) Applicants submit that the number of bits a CPU can process as a single unit (at one time) does not vary depending on whether the CPU is processing CISC instructions or RISC instructions, as taught by Blomgren1 and Blomgren2; namely, the largest number of bits which are handled as a single unit by a central processor of a digital computer or CPU is set based on the manufacturer of the processor/CPU.

Furthermore, Applicants submit that there is no suggestion as to any variation in the word sizes between the RISC and CISC instruction sets within either Blomgren1, Blomgren2 or the references of record, as described in Blomgren1:

> Two instruction decoders are required when the instruction sets are separate because the instruction sets each have an independent encoding of operations to opcodes. For example, both instruction sets have an ADD operation or instruction. However, the binary opcode number which encodes the ADD operation is different for the two instruction sets. In fact, the size and location of the opcode field in the instruction word is also different for the two instruction sets. In the x86 CISC instruction set, the opcode 03 hex is the ADD r,v operation or instruction for a long operand. This same opcode, 03 hex, corresponds to a completely different instruction in the PowerPC™ RISC instruction set. (Col. 1, lines 44-56.)

Likewise, as described in Blomgren2:

> A comparison of the opcode decoding of Table 2 for the RISC instruction set with Table 3 for the CISC instruction set shows that the two sets have independent encoding of instructions to opcodes. While both sets have ADD operations, the opcode number which encodes the ADD operation is different for the two instruction sets. In fact, the size and location of the opcode field in the instruction word is also different for the two instruction sets. (Col. 9, lines 16-20.) (Emphasis added.)

Applicants submit that although Huering and Jordan's Computer Systems Design and Architecture ("Huering") may suggest that the instruction sizes may vary between CISC and RISC instructions, the cited passages of Blomgren1 and Blomgren2 teach that the instruction word size is the same for both the CISC and RISC instruction sets, and in accordance with the definition of "word size" provide above. (See supra.) Unless the CISC and RISC instruction words are the same size, indication of "the size and location of the opcode field in the instruction word being different for the two instruction sets," as explicitly stated in both Blomgren1 and Blomgren2, makes no sense. In other words, use of the definite article in this context requires a single instruction word size. Accordingly, one skilled in the art would not interpret either Blomgren1 or Blomgren2 as teaching first and second ISAs having different word sizes, as recited by amended Claim 1.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" Lindemann Maschinenfabrik v. American Hoist & Derrick ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)*(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. Titanium Metals Corp. of American v. Banner ("Banner Titanium"), 778 F.2d 775, 777 (Fed. Cir. 1985).

Here, Applicants claim a multi-mode processor that includes a first instruction set architecture ISA having a first word size. The multi-mode processor also includes a second ISA having a second word size, the second word size being different than the first word size, as recited by amended Claim 1. As described at pg. 7 of Applicants' specification:

> In one embodiment, a processor is capable of operating in two modes. The first and second modes are a 32 bit word ISA and a 64 bit word ISA, respectively. More specifically, the first mode is IA-32 mode, in which a

> processor emulates a 32 bit word Intel Architecture (IA) known as IA-32 ISA . . . [T]he second mode is a IA-64, which implements what is known as the IA-64 ISA. (pg. 7, lines 1-16.) (Emphasis added.)

Accordingly, in one embodiment, the multi-mode processor provides backward compatibility or legacy support for a 32 bit word (legacy ISA), as well as support for a 64 bit word (current) ISA.

In contrast, Blomgren1 teaches the issuance of an unsupported opcode exception in response to detection of an unsupported CISC instruction and switches to an emulation mode when such an instruction is detected. The switch to the emulation mode results in the loading of an emulation routine including various RISC instructions to perform the CISC instruction. Once the exception handling is complete, the mode is switched to the CISC mode and a next CISC instruction is executed. (*See*, col. 14, lines 22-28.)

Likewise, Blomgren2 teaches the detection of an unknown opcode and switches to an emulation mode when such an instruction is detected. The switch to the emulation mode results in the loading of an emulation driver to perform the CISC instruction. Once completed, the emulation code returns control to the CISC mode, which causes a user program to continue execution with a next instruction. (*See*, col. 5, lines 57-65.)

Hence, Applicants submit that the entire specification of Blomgren1 and Blomgren2 are devoid of any reference to providing processing for different ISAs having different ISA word sizes. Applicants submit that the explicit text of Blomgren1 (*See*, col. 1, lines 44-56) and Blomgren2 (*See*, col. 9, lines 16-20) imply that the instruction word size is the same for both the CISC and RISC instruction sets, and in accordance with the definition of "word size" provide above.

Yet, in spite of the lack of any teaching toward processing of ISAs having a different word size, by improperly equating the term "instruction size" with the term "word size", the Examiner incorrectly finds a teaching within Blomgren1 and Blomgren2 to anticipate independent Claim 1.

Hence, Applicants respectfully submit that the Examiner is prohibited from relying on Blomgren1 and Blomgren2 as anticipatory references since the single prior art reference disclosure of Blomgren1 and Blomgren2 fail to exactly disclose each and every element recited by Claim 1. Banner Titanium, supra. Consequently, Applicants respectfully submit that Applicants' amendment to Claim 1 prohibits the Examiner from establishing prima facie case of anticipation since the single prior art reference disclosure of Blomgren1 and Blomgren2 fails to include the presence of each and every element recited by Claim 1, and as arranged in Claim 1. Lindermann, supra.

Therefore, Applicants respectfully submit that Claim 1, as amended, is patentable over Blomgren1 and Blomgren2. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 1, as well as dependent Claims 2-5 and 7-9.

Regarding Claim 10, Claim 10 is amended to recite the following claim feature which is neither taught not suggested by Blomgren1 and Blomgren2:

> if the processor is in a first word size instruction set architecture (ISA) mode, processing the input to render an arithmetic result;
> if the processor is in a second word size ISA mode, performing a token specific operation. (Emphasis added.)

As previously indicated, one embodiment of Applicants' Specification describes a processor that operates according to a 32-bit word ISA mode and a 64-bit word ISA mode (see Applicants' Specification pp. 7, lines 1-16.) As recited by amended Claim 10, a processor processes an input to render an arithmetic result if the processor is in a first word size ISA mode. As further recited by amended Claim 10, the processor performs a token specific operation if the processor is in a second word size ISA mode.

For at least the reasons provided above with regard to the §102(b) rejection of Claim 1, the word size referred to by the first word size ISA according to both Graf and the Computer Dictionary Online, in the context of a processor such as the method in a processor recited by amended Claim 10, the meaning of the term "word size" to one of ordinary skill

in the art at of computer architecture design, the time of invention, is the largest number of bits that a processor can process as a single unit (at one time.)

As indicated above, the number of bits that a CPU can process as a single unit (at one time) does not vary depending on whether the CPU is processing CISC instructions or RISC instructions, as taught by Blomgren1 and Blomgren2. Consequently, Applicants respectfully submit that neither the emulation mode nor the CISC mode taught by Blomgren1 and Blomgren2 disclose, teach or suggest the first word size ISA mode or the second word size ISA mode recited by amended Claim 10.

In contrast to the above recited features of amended Claim 10, Blomgren1 teaches the issuance of an unsupported opcode exception in response to detection of an unsupported CISC instruction and switches to an emulation mode when such an instruction is detected. The switch to the emulation mode results in the loading of an emulation routine including various RISC instructions to perform the CISC instruction. Once the exception handling is complete, the mode is switched to the CISC mode and a next CISC instruction is executed. (See, col. 14, lines 22-28.)

Likewise, Blomgren2 teaches the detection of an unknown opcode and switches to an emulation mode when such an instruction is detected. The switch to the emulation mode results in the loading of an emulation driver to perform the CISC instruction. Once completed, the emulation code returns control to the CISC mode, which causes a user program to continue execution with a next instruction. (See, col. 5, lines 57-65.)

In other words, both Blomgren1 and Blomgren2 teach the detection of an unknown opcode and switch to an emulation mode when such an opcode is detected. However, the passages cited by the Examiner, as well as the entire text of Blomgren1 and Blomgren2 are devoid of any reference to varying the processing of an input depending on whether the processor is in a first word size ISA mode or a second word size ISA mode, as recited by amended Claim 10. In contrast, Blomgren1 and Blomgren2 teach mode control logic that detects an unknown opcode which causes entry into emulation mode regardless of the processor mode. (See, Blomgren2, col. 7, lines 30-43.)

Accordingly, although Blomgren1 and Blomgren2 describe an emulation mode to emulate the unknown instruction, the processing performed within Blomgren1 and Blomgren2 does not vary according to a processor mode. Furthermore, even if assuming, arguendo, that Blomgren1 and Blomgren2 taught that the variation in processing of input depending on a processor mode, for at least the reasons provided above, the CISC mode and emulation modes taught by Blomgren1 and Blomgren2 neither teach nor suggest the first word size ISA mode or the second word size ISA mode. As recited by amended Claim 10, the first word size ISA refers a first word size that defines the largest number of bits handled as a single unit by a processor/CPU; the second word size ISA refers to a second word size that defines the largest number of bits which are handled as a single unit by a processor/CPU.

Accordingly, for at least the reasons provided above, Applicants respectfully submit that the Examiner is prohibited from relying on Blomgren1 and Blomgren2 as anticipatory references since each and every element recited by amended Claim 10 is not exactly disclosed by Blomgren1 and Blomgren2. Banner Titanium, supra. Consequently, Applicants respectfully submit that the Examiner fails to establish a prima facie case of anticipation since the Examiner fails to illustrate that the single prior art reference disclosure of Blomgren1 and Blomgren2 includes the presence of each and every element recited by amended Claim 10 and as arranged in amended Claim 10. Lindermann, supra.

Therefore, Applicants respectfully submit that Claim 10, as well as dependent Claims 11-13 and 15-17, base on their dependency from Claim 10, are also patentable over Blomgren1 as well as Blomgren2. Consequently, Applicants respectfully request that the examiner reconsider and withdraw the §102(b) rejection of Claims 10-13 and 15-17.

Regarding Claim 18, Claim 18 recites a multi-mode processor including the following claim feature which is neither disclosed, taught or suggested by Blomgren1 and Blomgren2:

> a plurality of instruction set engines to process instructions from a plurality of instruction set architectures, the plurality of instruction set architecture each having a different word size. (Emphasis added.)

Applicants respectfully submit that the above recited feature of amended Claim 18 is analogous to the previously recited feature of amended Claim 1. Accordingly, Applicants' arguments provided above with regard to the §102(b) rejection of Claim 1 equally apply to the §102(b) of Claim 18 as anticipated by Blomgren1 and Blomgren2.

The switching from a CISC mode to an emulation mode, whether based on an unsupported opcoded exception taught by Blomgren1 (see col. 14, lines 22-28) or the detection of an unknown opcode taught by Blomgren1 (see col. 15, lines 57-65,) to cause the switching to an emulation mode to perform various RISC instructions to perform the CISC instruction fails to disclose, teach or suggest a plurality of instruction set engines each having a different word size, as recited by amended Claim 18.

Therefore for at least the reasons provided above, Applicants respectfully submit that amended Claim 18 is patentable over Blomgren1 and Blomgren2 since Blomgren1 and Blomgren2 fail to disclose each and every element recited by Claim 18, and as arranged in Claim 18, as required to establish a prima facie case of anticipation. Lindermann, supra. Therefore, Applicants respectfully submit that Claim 18, as amended, is patentable over Blomgren1, as well as Blomgren2. Consequently Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 18.

Regarding Claim 19, Claim 19 recites a method of multi-mode processor including the following claim features which are neither disclosed, taught or suggested by Blomgren1 and Blomgren2:

> processing the input to render an arithmetic result when the processor is in at least a first word size instruction set architecture (ISA) mode of a plurality of word size ISA modes; and
>
> performing a token specific operation when the processor is in at least a second word size ISA mode of the plurality of word size (ISA) modes.

Applicants respectfully submit that the above recited features of amended Claim 19 are analogous to the previously recited features of Claim 10. Accordingly, Applicants' argument provided above with regard to the §102(b) rejection of Claim 10 equally applied to the §102(b) rejection of Claim 19 as anticipated by Blomgren1, and Blomgren2.

Accordingly, for at least the reasons provided above, Blomgren1 and Blomgren2 fail to disclose, teach or suggest the variation in processing of an input depending on a processor mode, as recited by amended Claim 19. Furthermore, the failure of Blomgren1 and Blomgren2 to disclose either a first word size ISA or a second word size ISA prohibits the Examiner from establishing that the single prior art reference disclosure of Blomgren1 and Blomgren2 includes the presence of each and every element recited by amended Claim 19, as arranged in Claim 19, and required to establish prima facie anticipation. Id.

Consequently, Applicants respectfully submit that Claim 19, as amended, is patentable over Blomgren1, as well as Blomgren2. Therefore, Applicants respectfully request that the examiner reconsider and withdraw the §102(b) rejection of Claim 19.

II. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejected Claims 6 and 14 under 35 U.S.C. §103(a) as being unpatentable over Blomgren1 and Blomgren2 in view of InstantWeb's Online Computing Dictionary terms "speculative evaluation" and "speculative execution" ("FOLDOC"). Applicants respectfully traverse this rejection.

Regarding the Examiner's citing of FOLDOC, Applicants respectfully submit that the Examiner's citing of FOLDOC fails to rectify the deficiencies of Blomgren1 and Blomgren2 in either teaching or suggesting ISAs having different word sizes, as recited by amended Claim 1, or a variation in processing of input depending on a processor mode, as recited by amended Claim 10. Therefore, for at least the reasons provided above, Applicants respectfully submit that Claims 1 and 10 are patentable over the combination of Blomgren1 and Blomgren2 in view of FOLDOC.

Therefore, for at least the reasons provided above, Claim 6 and 14, based on their dependencies from Claim 1 and 10, respectively, are also patentable over the combination of Blomgren1 and Blomgren2 in view of FOLDOC. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 6 and 14.

The Patent Office rejected Claim 18 under 35 U.S.C. §103(a) as being unpatentable over Blomgren1 and Blomgren2 in view of The Microarchitecture of Pipelined and Superscalar Computers by Amos Omondi, © 1999 ("Omondi"). Applicants respectfully traverse this rejection.

Regarding the Examiner's citing of Omondi, Applicants respectfully submit that the Examiner's citing of Omondi fails to rectify the deficiencies of Blomgren1 and Blomgren2 in teaching or suggesting a plurality of instruction set architectures each having a different word size. Consequently, for at least the reasons provided above, Applicants respectfully submit that Claim 18, as amended, is patentable over the prior art combination of Blomgren1 and Blomgren2 in view of Omondi. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 18.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-19, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: October 30, 2006

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage on the date below, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Annie McNally — 10/30/2006
Annie McNally — Date